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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/759,819
Filing Date: January 16, 2004
Appellant(s): HAYDEN, DOUGLAS TODD

Philip S. Lyren
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed January 30, 2007 appealing from the Office action mailed September 14, 2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

A substantially correct copy of appealed claims 1-7, 9-11 and 31-36 appears on page 11 of the Appendix to the appellant's brief. The minor errors are as follows: The status of claims 1-7 and 9-11 should read as Original and the status of claims 31-36 should read as Previously Presented.

(8) Evidence Relied Upon

5,729,062	Satoh	03-1998
5,644,731	Liencres et al.	07-1997

Phillips Semiconductors; "The I2C-Bus Specification"; Phillips Semiconductors; Revision 2.1; January 2000; all pages.

Li, Paul; "LVTC Logic family for live-insertion using standard CMOS process"; Pericom Semiconductor; January, 24, 2003; pages 1-3.

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-6, 9-10, 31-33 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Satoh (US 5,729,062).

For claim 1 Satoh teaches:

A system comprising:

- a bus comprising signal lines (Fig. 5, items 15a and 15b; col. 4, ll. 38-50); and
- a device (Fig. 9, item 5) configured to be inserted onto and removed from the bus through contacts (Fig. 9, items 57-59) configured to provide at different times during insertion

and removal contact between a pre-charge circuit and one of the signal lines, and a low-impedance across the pre-charge circuit (col. 5, line 62 – col. 6, line 27).

While Satoh discloses contacts configured to provide at different times during insertion and removal contact between a pre-charge circuit and a power supply line, and a low-impedance across the pre-charge circuit, Satoh does not expressly disclose such a pre-charge circuit and a low-impedance short circuit on the bus signal lines 15a and 15b of figure 5. Satoh however admits, "Various modifications will become possible for those skilled in the art after receiving the teachings of the present disclosure without departing from the scope thereof (col. 7, ll. 1-3)." With regards to the teachings of Satoh, it is disclosed that implementing the invention of Satoh "...limits a rush current to flow when the power source pin 57 of the package connecter is connected to the terminal of the mother board connecter..." (col. 6, ll. 18-20) and "...reduces the variation of the power source current to occur when the power source pin 19 of the package connector 18 is connected to the mother board connector and on the transition from the plug-in mode to the regular mode. Consequently, the package connector 18, mother board connector 24 and wirings are free from damage (col. 6, ll. 43-48)."

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to apply the active plug-in circuit used to limit the in-rush current on the power supply line of figure 9 on the bus signal lines of figure 5 such that the in-rush current flow across the bus signal lines is reduced thus resulting in a device who's connector is free from damage.

Fig. 5

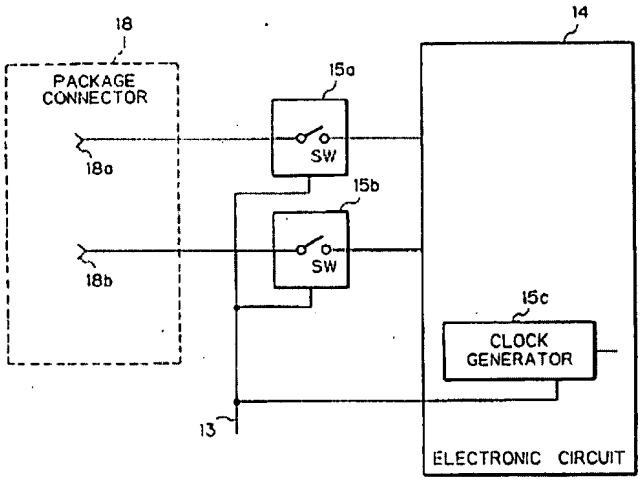
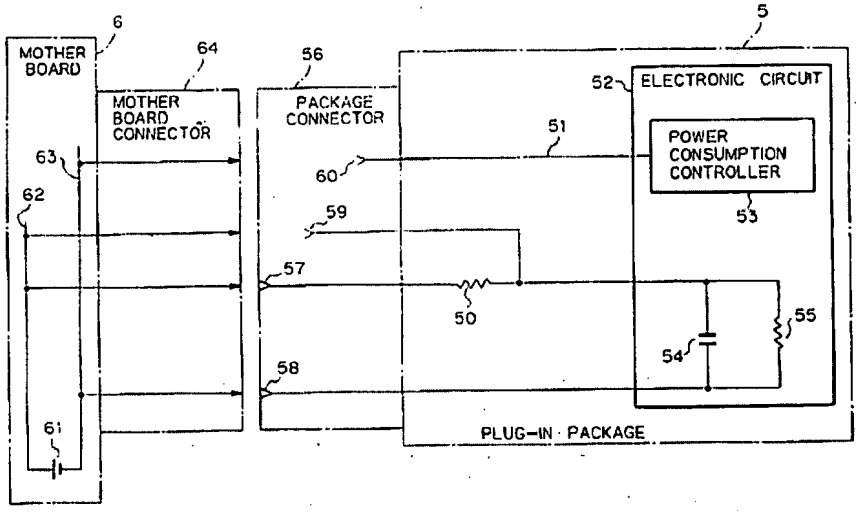

18
PACKAGE CONNECTOR
18a
18b
15a
SW
15b
SW
14
15c
CLOCK GENERATOR
13
ELECTRONIC CIRCUIT

Fig. 9


6
MOTHER BOARD
64
MOTHER BOARD CONNECTOR
63
62
61
56
PACKAGE CONNECTOR
60
59
57
58
50
5
52
ELECTRONIC CIRCUIT
51
POWER CONSUMPTION CONTROLLER
53
54
55
PLUG-IN PACKAGE

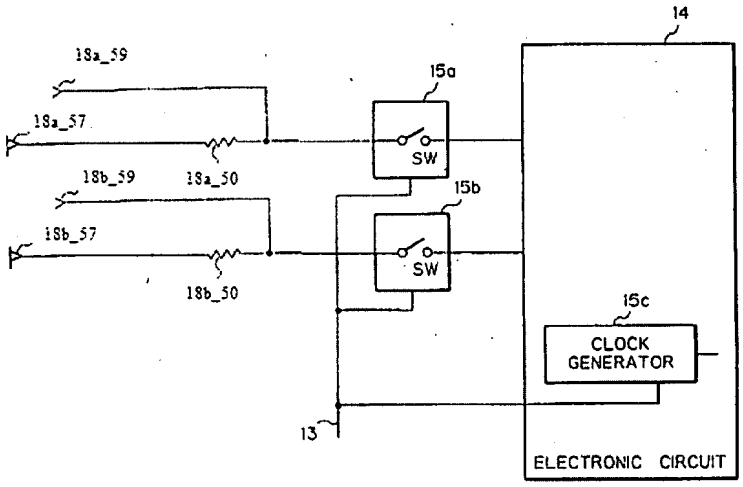


Fig. 5 in view of Fig. 9

The combination of figures 9 and 5 (shown above) would thus result in each of bus signal line connectors 18a and 18b having connectors 57 and 59 of figure 9. In other words, bus signal line 18a would be replaced with contacts 59 and 57 of figure 9 (Shown in the illustrative drawing Fig. 5 in view of Fig. 9 as contacts 18a_59 and 18a_57) thus providing the bus signal line of the motherboard with current limiting circuit (resistor 50 of Fig. 9; Shown in the illustrative drawing Fig. 5 in view of Fig. 9 as 18a_50) and the low-impedance short circuit (Shown in the illustrative drawing Fig. 5 in view of Fig. 9 as the signal line connected to pin 18a_57). Likewise, bus signal line 18b would be replaced with its own contact 59 and 57 of figure 9 (Shown in the illustrative drawing Fig. 5 in view of Fig. 9 as contacts 18b_59 and 18b_57) thus providing that bus signal line of the motherboard with current limiting circuit (resistor 50 of Fig. 9; Shown in the illustrative drawing Fig. 5 in view of Fig. 9 as 18b_50) and the low-impedance short circuit (Shown in the illustrative drawing Fig. 5 in view of Fig. 9 as the signal line connected to pin 18b_57). Therefore the low-impedance short circuit and the current limiting circuit of each bus signal line 18a and 18b would be placed in series prior to the switches 15a and 15b since low-

impedance short circuit and current limiting circuit are show in figure 9 to the first elements connected to the mother board connector 64 (As shown in the illustrative drawing Fig. 5 in view of Fig. 9).

For claim 2 Satoh teaches:

The system of claim 1, where the pre-charge circuit comprises a resistor located between one of the contacts and the device (Fig. 9, item 50; col. 6, ll. 18-20).

For claim 3 Satoh teaches:

The system of claim 1, comprising a switch located between the contacts and the device (Fig. 5, items 15a and 15b; col. 4, ll. 38-50; the switches close only when the bus signal lines have been stabilized).

For claim 4 Satoh teaches:

The system of claim 3, where the switch is a field effect transistor located between the contacts and the device.

Satoh teaches that the switches (Fig. 5, 15a and 15b) are electronically controlled by the output of mode setting device 12 (Fig. 3) but does not explicitly state the switches are field effect transistors. Furthermore, Satoh admits knowledge of CMOS (Complimentary Metal Oxide Semiconductor) field effect transistors and their low power consumption (col. 4, ll. 51-57). As such *Official Notice* is taken that the use of field effect transistors as switching devices is well known to those skilled in the art.

For claim 5 Satoh teaches:

The system of claim 3, where the switch is configured to conduct after the low-impedance is provided across the pre-charge circuit (The switches 15a and 15b are closed only when the electronic circuit is stabilized as a result of the low impedance circuit [Fig. 9] connecting to the mother signal line [col. 4, ll. 38-50]).

For claim 6 Satoh teaches:

The system of claim 1, comprising reference contacts configured to provide a common reference to the bus and the device before contact between the pre-charge circuit and one of the signal lines as the device is inserted onto the bus (Fig. 9, item 63).

For claim 9 Satoh teaches:

The system of claim 1, comprising power contacts, where the power contacts are configured to provide power at the same time as contact between, the pre-charge circuit and one of the signal lines, as the device is inserted onto the bus (Since the teachings of the power contacts is applied to the bus signal lines the power contacts and the bus signal contacts would thus connect at the same time).

For claim 10 Satoh teaches:

The system of claim 1, where the signal lines comprise a serial data line and a serial clock line (col. 4, ll. 38-50).

For claim 31 Satoh teaches:

A system, comprising:

- a bus comprising signal lines (Illustrative drawing Fig. 5 in view of Fig. 9 above, lines just to items 15a and 15b; col. 4, ll. 38-50);
- a device configured to be inserted onto and removed from the bus (Fig. 3, item 1) through contacts (Illustrative drawing Fig. 5 in view of Fig. 9 above, items 18_57 and 18_59) configured to provide at different times during insertion and removal contact between a pre-charge circuit and one of the signal lines, and a low-impedance across the pre-charge circuit (col. 5, line 62 – col. 6, line 27; please see rejection of claim 1 above),
- the contacts comprising a connector system including a first connector (Illustrative drawing Fig. 5 in view of Fig. 9 above, 18a_57; please see rejection of claim 1 above), a second connector (Illustrative drawing Fig. 5 in view of Fig. 9 above, 18a_59; please see rejection of claim 1 above), where the first connector is configured to provide a first pre-charge circuit between the second connector and a first bus signal line and the second connector is configured to provide a first short-circuit between the second connector and the first bus signal line, where the first connector and the second connector are staggered to provide the first pre-charge circuit and the first short-circuit at different times during engagement and disengagement of the connector system (col. 5, line 62 – col. 6, line 27; please see rejection of claim 1 above).

For claim 32 Satoh teaches:

The system of claim 31comprising:

- a third connector (Illustrative drawing Fig. 5 in view of Fig. 9 above, 18b_57; please see rejection of claim 1 above); and
- a fourth connector (Illustrative drawing Fig. 5 in view of Fig. 9 above, 18b_59; please see rejection of claim 1 above) where the third connector is configured to provide a second pre-charge circuit between the fourth connector and a second bus signal line, and the fourth connector is configured to provide a second short-circuit between the fourth connector and the second bus signal line, where the third connector and the fourth connector are staggered to provide the second pre-charge circuit and the second short-circuit at different times during engagement and disengagement of the connector system (col. 5, line 62 – col. 6, line 27; please see rejection of claim 1 above).

For claim 33 Satoh teaches:

The system of claim 32, where the first connector and the third connector are staggered to simultaneously provide the first pre-charge circuit between the second connector and the first bus signal line and the second pre-charge circuit between the fourth connector and the second bus signal line (Since the teachings of the power contacts is applied to both bus signal lines the connections associated with each bus signal would connect at the same time).

For claim 35 Satoh teaches:

The system of claim 33, where the second connector and the fourth connector are staggered to simultaneously provide the first short-circuit between the second connector and the first bus

signal line, and the second short-circuit between the fourth connector and the second bus signal line (Since the teachings of the power contacts is applied to both bus signal lines the connections associated with each bus signal would connect at the same time).

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Satoh as applied to claim 1 above, and further in view of Paul Li.

Satoh teaches a hot-insertion system (please see the rejection of claim 1 above) in which the power and reference lines connect at substantially equivalent times. Satoh does not expressly state implementing a staggered connection of power and reference lines.

Li teaches (page 3):

The major design guideline for hot-swap is that during hot-swapping, connect the ground pin of the inserting card to the ground pin of the motherboard before any other signal or power pins are connected. This is the main request for hot-swap. It is the industry standard for any hot-swap applications for both logic and switch devices. If the ground pins of the card and motherboard were not connected before any other pins during hot-swap, the voltage of the power and signal at connectors will go wild due to the lack of ground reference, and will burn the logic device designed for hot-swap.

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to stagger the connection of the ground and power pins of Satoh such that voltages will not go wild due to lack of ground reference and will not burn the logic device.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Satoh as applied to claim 1 above, and further in view of The I²C Specification.

Satoh teaches the bus signal lines comprising a singular data line along with a clock signal much like an inter-integrated circuit (I^2C) bus but does not explicitly state the two bus signal lines represent an I^2C bus.

The I²C Specification teaches the I²C is an excellent choice for device communication because:

- Only two bus lines are required; a serial data line (SDA) and a serial clock line (SCL)
- Each device connected to the bus is software addressable by a unique address and simple master/slave relationships exist at all times; masters can operate as master-transmitters or as master-receivers
- Design-time reduces as designers quickly become familiar with the frequently used functional blocks represented by I2C-bus compatible ICs
- ICs can be added to or removed from a system without affecting any other circuits on the bus
- Fault diagnosis and debugging are simple; malfunctions can be immediately traced (page 4)

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to implement the data and signal line of Satoh as an I²C bus because the simple 2-wire serial I2C-bus minimizes interconnections so ICs have fewer pins and there are not so many PCB tracks resulting in - smaller and less expensive PCBs.

Claims 34 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Satoh as applied to claim 1 above, and further in view of Liencres et al. (US 5,644,731).

Satoh teaches a hot insertion system (please see the rejection of claim 1 above) where the connection of a data signal line 18b (Fig. 5) and a clock signal line 18a (Fig. 5) occur at a substantially equivalent. Satoh does not expressly teach that the connection of the clock and data signal lines can be staggered in a sequence.

Liencres teaches a hot insertion system similar to Satoh in that the connection of a plurality of bus signal lines (Fig. 3A, 3213a – 3213n; Fig. 4A, 4213a – 4213n) occur at a substantially equivalent time. In addition to this similar hot insertion system Liencres also teaches using convex and concave connectors (Fig. 5A and 5B) such that bus signal lines are connected in a staggered fashion. It is important to note however that the operations of the interfaces (both the simultaneous connection as shown in Fig. 3A and the staggered connections of Fig. 5A and 5B) are similar (col. 7, ll. 1-7) but the convex and concave connectors provide a shape that enhances immunity to a tilted insertion.

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to implement the convex or concave connector of Liencres into the hot-insertion system of Satoh such that the Plug-In package of Satoh is provided with staggered bus signal connections that enhance the immunity of a tilted card insertion.

(10) Response to Argument

Applicant's arguments regarding independent claim 1 and all dependent claims are summarized by three examples (see Appeal Brief, pages 6-7):

- (1) "Notice that nowhere does Satoh teach or suggest that contacts between a pre-charge circuit and a signal line engage at different times."
- (2) "Satoh does discuss a low power consumption mode in connection with Fig. 5 (see col. 4, lines 38-39), but nowhere does Satoh suggest 'a low-impedance across the pre-charge circuit.'"
- (3) "Applicant respectfully assert that a generalization on various modifications in Satoh is not sufficient to suggest to one skilled in the art a specific embodiment (i.e., the embodiment recited in the claims). The Examiner has provided no explanation whatsoever as to explain why one of ordinary skill in the art at the time the invention was made would have been motivated to make the proposed modification based merely on a generalization in Satoh."

Regarding example one (1), the Examiner has shown in the rejection of claim 1 that one of ordinary skill in the art at the time the invention was made would have found it obvious to incorporate the teaching of Fig. 9 into Fig. 5 (achieving illustrative drawing Fig. 5 in view of Fig. 9 above) such that the use of pre-charge circuit 18a_50 (or 18b_50) "limits a rush to flow when the" bus signal "is connected to the terminal of the mother board connector" (Satoh; col. 6, ll. 18-20) and thus "the package connector 18, mother board connector 24 and wiring are free from damage" (Satoh; col. 6, ll. 47-48). The combination of Fig. 5 in view of Fig. 9 (illustrated above) clearly shows the pre-charge circuit contact 18a_57 makes contact with the motherboard connector prior to signal line contact 18a_59 based on the length of the contacts. As such applicant's first example is not persuasive to overcome the rejection.

Regarding example two (2), the combination of Fig. 5 in view of Fig. 9 clearly shows the signal contact line 18a_59, representing the low-impedance path, is provided across the pre-charge circuit when the contact 18a_59 mates with the motherboard connector. As such applicant's second example is not persuasive to overcome the rejection.

Regarding example three (3), the Examiner has previously maintained (see page 4 of Examiner Answer) "With regards to the teachings of Satoh, it is disclosed that implementing the invention of Satoh "...limits a rush current to flow when the power source pin 57 of the package connecter is connected to the terminal of the mother board connecter..." (col. 6, ll. 18-20) and "...reduces the variation of the power source current to occur when the power source pin 19 of the package connector 18 is connected to the mother board connector and on the transition from the plug-in

mode to the regular mode. Consequently, the package connector 18, mother board connector 24 and wirings are free from damage (col. 6, ll. 43-48).”” Therefore, contrary to applicant's assertion, the Examiner has provided motivation as to why one of ordinary skill in the art at the time the invention was made would have been motivated to make the proposed modification based merely on a generalization in Satoh. As such applicant's third example is not persuasive to overcome the rejection.

Applicant's arguments regarding independent claim 31 and all dependent claims are summarized by six examples (see Appeal Brief, pages 7-9):

- (1) to (3) and (6) are similar to points (1) to (3) and (1) for claim 1 and are not persuasive for the reasons discussed above.
- (4) “...where does Satoh teach or suggest two connectors where the first connector is configured to provide a first pre-charge circuit between the second connector and a first bus signal line?”
- (5) “Where is a second conductor that provides a short-circuit between itself and a bus-line?”

Regarding example four (4), the rejection of independent claim 31 reads as follows:

> the contacts comprising a connector system including a first connector (Illustrative drawing Fig. 5 in view of Fig. 9 above, 18a_57; please see rejection of claim 1 above), a second connector (Illustrative drawing Fig. 5 in view of Fig. 9 above, 18a_59; please see rejection of claim 1 above), where the first connector is configured to provide a first pre-charge circuit between the second connector and a first bus signal line and the second connector is configured to provide a first short-circuit between the second connector and the first bus signal line, where the first connector and the second connector are staggered to provide the first pre-charge circuit and the first short-circuit at different times during

engagement and disengagement of the connector system (col. 5, line 62 – col. 6, line 27; please see rejection of claim 1 above).

Therefore, the combination of Fig. 5 in view of Fig. 9 (as illustrated above) shows the first connector 18a_57 and second connector 18a_59. As such applicant's fourth example is not persuasive to overcome the rejection.

Regarding example five (5), the rejection of independent claim 31 reads as follows:

the contacts comprising a connector system including a first connector (Illustrative drawing Fig. 5 in view of Fig. 9 above, 18a_57; please see rejection of claim 1 above), a second connector (Illustrative drawing Fig. 5 in view of Fig. 9 above, 18a_59; please see rejection of claim 1 above), where the first connector is configured to provide a first pre-charge circuit between the second connector and a first bus signal line and the second connector is configured to provide a first short-circuit between the second connector and the first bus signal line, where the first connector and the second connector are staggered to provide the first pre-charge circuit and the first short-circuit at different times during engagement and disengagement of the connector system (col. 5, line 62 – col. 6, line 27; please see rejection of claim 1 above).

Therefore, the combination of Fig. 5 in view of Fig. 9 (as illustrated above) shows the second connector 18a_59 provides a short-circuit between itself and a bus-line. As such applicant's fifth example is not persuasive to overcome the rejection.

Regarding the rejection of dependent claim 4, *Official Notice* was taken to state that the use of field effect transistors as switching devices is well known to those skilled in the art at the time of applicant's invention. Applicant has not traversed the Examiner use of *Official Notice* and the use of field effect transistors as switching devices is taken to be admitted prior art. See MPEP §2144.03 C:

"If applicant does not traverse the examiner's assertion of official notice or applicant's traverse is not adequate, the examiner should clearly indicate in the next Office action that the common knowledge or well-known in the art statement is taken to be admitted prior art because applicant either failed to traverse the examiner's assertion of official notice or that the traverse was inadequate."

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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